Tutorial 4 - SS2016
Communication Systems and Protocols

Institute for Information Processing Technologies - ITIV
Dr.-Ing. Jens Becker • Dipl.-Inform. Tanja Harbaum

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Task 1: I^{2}C-Bus Synchronization

Three I^{2}C Bus Masters want to send data to one slave. Each node needs one time step to read in data from external signal lines (SCL, SDA). The reaction time within each node is neglectably small (0 time steps). The individual masters want to establish a clock signal according to the following table 1.1:

Master	Low period	High period
A	8	4
B	4	12
C	12	8

Table 1.1: clock signals

Assume that Master B is initiating the communication cycle.

A) In general, which functionality does the I^{2}C bus provide for the case that multiple master nodes want to communicate at the same time with the same slave node?

1

The I^{2}C-Bus uses clock synchronization and arbitration (over the complete dataframe, over address and data fields).

B) Complete the waveforms of the signals that result from the interaction between the nodes on the SCL signal.

3

C) In general, which functionality does the I2C bus provide for the case of a master node needing to communicate with a slower slave node?

2

The I^{2}C-Bus uses a kind of handshake mechanism that allows slave nodes to insert wait states if the master provides new data too fast. The wait state insertion is controlled by the SCL signal. In general, the SCL signal is generated by a wired-AND connection with dominant "0" of the participants CLK signals. A wait state is inserted if the SCL signal remains "LOW" and is initiated by a slave.
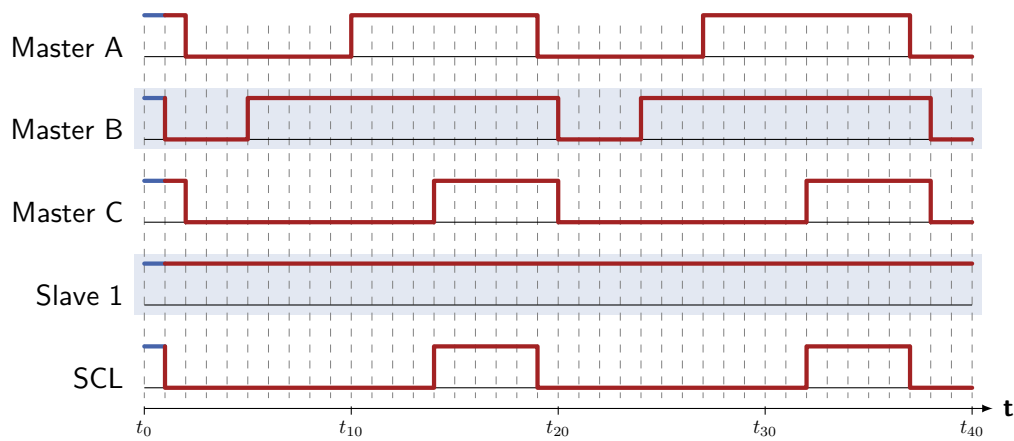
Figure 1.1: Signal sequence

8

Task 2: Cyclic Redundancy Check

Task 2.1: Transmission

To protect a data transmission, CRC with the generator polynomial $g(x) = x^2 + 1$ is used.

A) Determine the bit string that is associated with the generator polynomial.

1

Polynomial Generator: $1 \cdot x^2 + 0 \cdot x^1 + 1 \cdot x^0 \rightarrow$ Bitstring: 1 0 1

B) What is the length of the checksum that is to be appended to the data stream?

1

Length of the checksum = Order of polynomial generator. here: order $g(x) = 2$

C) c) Calculate the data stream that will be transmitted if the following bit string is to be protected: 1001010101.

2

```
1  0  0  1  0  1  0  1  0  1  0  0      :      1  0  1
1  0  1
0  0  1  1  0
      1  0  1
      0  1  1  1
         1  0  1
         0  1  0  0
            1  0  1
            0  0  1  1  0
                  1  0  1
                  0  1  1  1
                     1  0  1
                     0  1  0  0
                        1  0  1
                        0  0  1  0   remainder
```

Bit string to be transmitted: 1001010101 10

Task 2.2:   Reception

In a transmission system that uses CRC for error protection, a sender transmits the following bit stream: 100101010110. Due to interferences during transmission the last 4 bits of the bit stream are flipped before reaching the receiving node.

A)   Denote the bit stream as it arrives at the receiving node.

Received bit stream: 100101011001

> **1**

B)   Carry out the CRC error detection scheme of the receiver assuming that the generator polynomial $g(x) = x2 + 1$ has been used.
What does the receiver conclude from the result? Explain and discuss the reasons for the receiver's conclusion.

> **2**

$$
\begin{array}{ccccccccccccc}
1 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 1 & 0 & 0 & 1 & \quad : \quad 1 \; 0 \; 1 \\
1 & 0 & 1 \\
\hline
0 & 0 & 1 & 1 & 0 \\
 & & 1 & 0 & 1 \\
\hline
 & & 0 & 1 & 1 & 1 \\
 & & & 1 & 0 & 1 \\
\hline
 & & & 0 & 1 & 0 & 0 \\
 & & & & 1 & 0 & 1 \\
\hline
 & & & & 0 & 0 & 1 & 1 & 1 \\
 & & & & & & 1 & 0 & 1 \\
\hline
 & & & & & & 0 & 1 & 0 & 0 \\
 & & & & & & & 1 & 0 & 1 \\
\hline
 & & & & & & & 0 & 0 & 1 & 0 & 1 \\
 & & & & & & & & & 1 & 0 & 1 \\
\hline
 & & & & & & & & & 0 & 0 & 0 & \text{remainder}
\end{array}
$$

Generator polynomial is too short to detect a burst error of length 4.

Task 2.3: Hardware implementation

A) To protect data transmissions in a mobile device, the CRC scheme is to be implemented using linear feedback registers with XOR operations. Draw the simplified hardware layout for the polynomial CRC-12 ($x^{12} + x^{11} + x^3 + x^2 + x + 1$).

1

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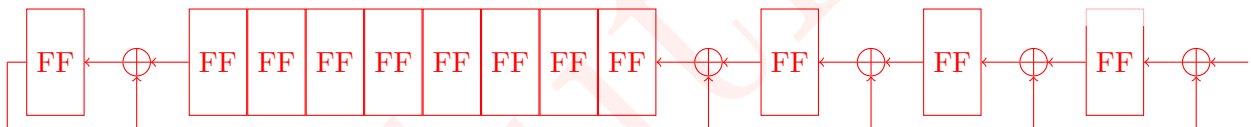
Task 3: Actuator Sensor Interface (ASI)

In the following a data transmission on the ASI bus is considered. Thereby a master wants to transmit the bit vector 01001 to the slave having address 26_d. The telegram format of the ASI bus is shown in Figure 3.1.

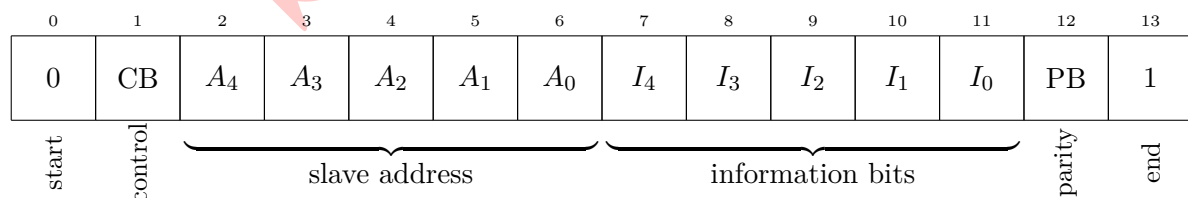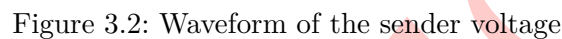| 0	1	2	3	4	5	6	7	8	9	10	11	12	13
0	CB	A_4	A_3	A_2	A_1	A_0	I_4	I_3	I_2	I_1	I_0	PB	1
start	control			slave address					information bits			parity	end

Figure 3.1: ASI packet format, master call

A) Specify the course of the sender voltage on the ASI bus. A time offset does not need to be considered (Note: The control bit must have value '0' for data transmission, use even parity without considering start / stop bits). Use figure 3.2 and Manchester as per IEEE 802.3
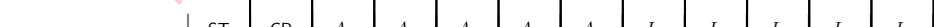
3

Figure 3.2: Waveform of the sender voltage

B) Figure 3.3 shows the waveform on the ASI bus when transmitting a master call. Due to external influences the transmission has been disturbed. Mark the errors and name the rule(s) by which they are detected.

3

1. Start and stop bits: first impulse has to be negative, last impulse has to be positive
2. Succeeding impulses must have different polarity
3. Between two impulses of a telegram the pause that is allowed lasts half a bit time at maximum
4. The parity of the telegram must be even. In the example this cannot be seen since the transmitted data cannot be reconstructed due to the great amount of errors

Figure 3.3: Waveform of the sender voltage

Task 4: I^{2}C-Bus Arbitration

The frame format of I^{2}C-bus is shown in figure 4.1. Three master nodes are simultaneously trying to transmit one byte of data to different slaves over the I^{2}C-bus.

S	slave address	$R/\bar{W}$	A	DATA	A	DATA	$A/\bar{A}$	P

data transfered (n bytes + acknowledge)
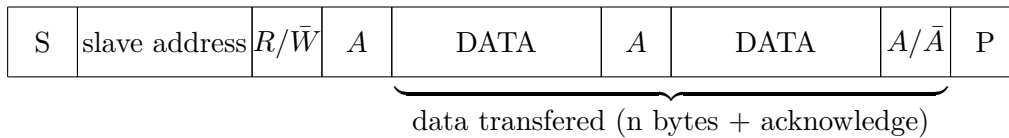
term	descripion
S	start condition
slave address	7-bit slave address
$R/\bar{W}$	read/write: read 1, write 0
A	acknowledge from slave
$\bar{A}$	not acknowledge
DATA	8-bit data
P	stop Condition

Figure 4.1: I^{2}C-bus frame format

A) The addresses of the slaves and the data to be send to them is shown in the table 4.1. Complete the signal diagram in the figure 4.2.
Hint: A slave always answers with a positive Acknowledge (0).

node	slave address	data
Master 1	0100110	00011010
Master 2	0100101	10100111
Master 3	0100101	00101101

Table 4.1: test

B) Which node is winning the arbitration?

Node 3 is winning arbitration

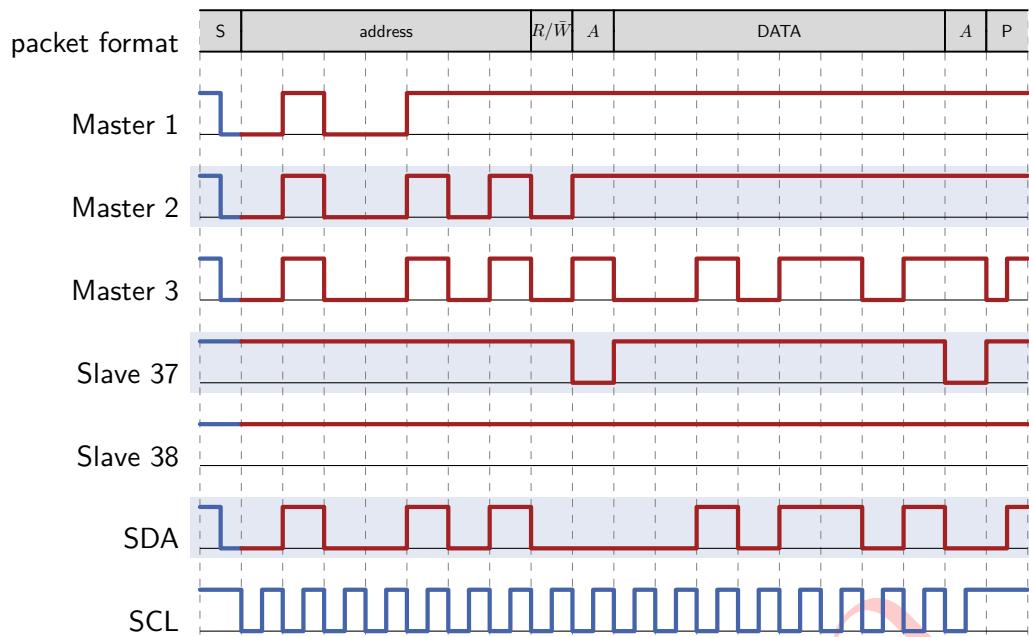C) Can an I^{2}C master node change the priority of a slave node during runtime of the system?

Figure 4.2: Signal sequence

Normally slaves are prioritized by their address in the system. These are predefined during design time of the system and are fixed. Therefore the master cannot change their priorities.

If no hardwired coding is used with the slave, a slave can be reconfigured with the general call address and its address be changed